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10CS33

Third Semester B.E. Degree Examination, December 2012
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO questions from each part.***

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – A

1 a. Differentiate analog and digital signals. Define period, frequency and duty cycle of a digital signal. Prove that the duty cycle of a symmetrical waveform is 50%. **(06 Marks)**

b. What are universal gates? Realize $\left(\overline{(A+B)}\cdot C\right)$ using only NAND gates. **(05 Marks)**

c. Describe positive and negative logic. List the equivalences between them. **(04 Marks)**

d. What is the need for HDL? Explain the structure of VHDL / verilog program. **(05 Marks)**

2 a. Find the minimal SOP of the following Boolean functions using K-Maps:

i) $f(a, b, c, d) = \sum m(6,7,9,10,13) + d(1,4,5,11)$

ii) $f(w, x, y, z) = \pi m(1,2,3,4,9,10) + d(0,1,4,15)$ **(08 Marks)**

b. Simplify $f(A, B, C, D) = \sum m(0,1,2,3,10,11,12,13,14,15)$ using Quine-Mc Clusky method. **(08 Marks)**

c. What are static hazards? How to design a hazard free circuit? Explain with an example. **(04 Marks)**

3 a. Design and implement BCD to excess-3 code converter using four 8:1 multiplexers. Take MSB 'A' as map entered variable (input variable) 'BCD' lines as select lines, assuming f(A, B, C, D) as BCD input. **(08 Marks)**

b. Realize a logic circuit for Octal to binary encoder. **(06 Marks)**

c. Draw the PLA circuit and realize the Boolean functions: $X = A'B'C + AB'C' + B'C$, $Y = A'B'C + AB'C'$, $Z = B'C$ **(04 Marks)**

d. Give the HDL implementation of 2:1 MUX. **(02 Marks)**

4 a. Draw the logic diagram, truth table and timing diagram for edge-triggered D-flip flop. **(06 Marks)**

b. With a neat logic diagram and truth table, explain the working of JK Master-Slave Flip-Flop along with its implementation using NAND gates. **(06 Marks)**

c. Analyze the behavior of the sequential circuit shown in Fig. Q4 (c) and draw the state table and state transition diagram. **(08 Marks)**

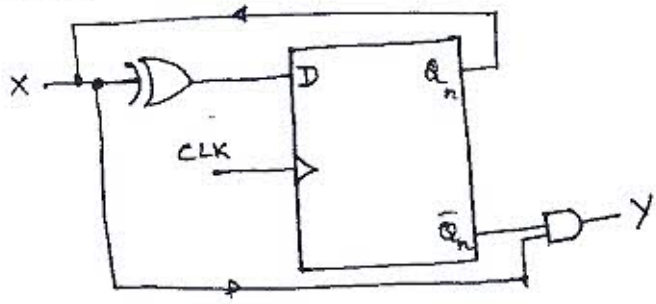

Fig. Q4 (c)

PART – B

5 a. Using positive edge triggered D flip-flops, draw the logic diagram for a 4-bit parallel-in-serial-out (PISO) shift register and explain its working to load 1001 into it and shift the same. **(08 Marks)**

b. With a neat diagram, explain how shift registers can be applied for serial addition. **(05 Marks)**

c. How long will it take to shift an 4 bit number into 4 bit PISO shift register that operates at clock frequency of 5 MHz. Also, what is the time required to extract 4-bit number from PISO operates at 5 MHz clock? **(04 Marks)**

d. Write verilog/VHDL code for Johnson counter. **(03 Marks)**

6 a. With the help of neat block diagram and timing diagram, explain the working of a Mod-16 ripple counter constructed using positive edge triggered JK flip-flops. **(08 Marks)**

b. Design a self-correcting Mod-5 synchronous down counter using JK flip-flops. Assume 100 as the next state for all the unused states. **(08 Marks)**

c. List any two drawbacks of asynchronous counter. What is the clock frequency in a 3-bit counter, if the clock period of the waveform at last flip-flop is 24 μs? **(04 Marks)**

7 a. How does state transition diagram of a Moore machine differ from Mealy machine? Draw the state transition diagram of synchronous sequential logic circuit using Mealy model that detects three consecutive zeros from an input data stream, X and signals detection by making output, Y = 1. **(06 Marks)**

b. Draw the ASM chart for vending machine problem using Mealy model. **(08 Marks)**

c. What is the use of state reduction technique? Demonstrate the state reduction by implication table method. **(06 Marks)**

8 a. With a neat diagram, explain the working of a 4-bit D/A converter. **(08 Marks)**

b. What is the accuracy and resolution of an 8-bit D/A converter? Find the resolution and accuracy of the same if the full scale output is +10V. **(04 Marks)**

c. Discuss the working of following A/D converters:

i) Successive approximation A/D.

ii) Counter type A/D. **(08 Marks)**

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