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Third Semester B.E. Degree Examination, Dec.2014/Jan.2015
Logic Design

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

- 1 a. What are universal gates? Realize $\overline{(A+B)} \cdot \overline{(A+B)}$ using only universal gates. (05 Marks)
- b. Discuss the positive and negative logic and list the equivalences in positive and negative logic. (05 Marks)
- c. An asymmetrical signal waveform is high for 2 m sec and low for 3 m sec. Find
i) Frequency ii) Period iii) Duty cycle low iv) Duty cycle high. (05 Marks)
- d. Explain the structure of VHDL / Verilog program. (05 Marks)
- 2 a. The system has four inputs, the output will be high only when the majority of the inputs are high. Find the following :
i) Give the truth table and simplify by using K-map.
ii) Boolean expression in $\sum m$ and $\prod M$ form.
iii) Implement the simplified equation using NAND – NAND gates and NOR – NOR gates. (10 Marks)
- b. Find essential prime implicants for the Boolean expression by using Quine – Mc Clusky method.
 $f(A, B, C, D) = \sum m(1, 3, 6, 7, 9, 10, 12, 13, 14, 15)$. (10 Marks)
- 3 a. Implement the Boolean function expressed by SOP :
 $f(A, B, C, D) = \sum m(1, 2, 5, 6, 9, 12)$ using 8 – to – 1 MUX. (06 Marks)
- b. Implement a full adder using a 3 – to – 8 decoder. (06 Marks)
- c. Design 7 – segments decoder using PLA. (08 Marks)
- 4 a. Give state transition diagram of SR, D, JK and T Flip – Flop. (06 Marks)
- b. With a neat logic diagram and truth table, explain the working of JK Master – Slave Flip – Flop along with its implementation using NAND gates. (07 Marks)
- c. Show how a D Flip – Flop can be converted into JK Flip – Flop. (07 Marks)

PART – B

- 5 a. With a neat logic and timing diagram, explain the working of a 4-bit SISO register. (10 Marks)
- b. Design two 4-bit serial Adder. (06 Marks)
- c. Write the verilog code for switched tail counter using “assign” and “always” statement. (04 Marks)
- 6 a. Design synchronous mod-5 UP counter using JK Flip-Flop. (10 Marks)
- b. Explain a 3-bit binary Ripple down counter, give the block diagram, truth table and output waveforms. (10 Marks)

- 7 a. With a neat block diagram, explain Mealy and Moore model. (10 Marks)
 b. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig. Q7 (b). (10 Marks)

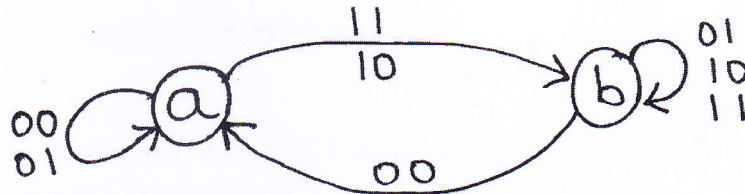


Fig. Q7 (b)

- 8 a. Explain the R/2R Ladder technique of D/A conversion. (10 Marks)
 b. Explain with neat diagram, single slope A/D converters. (10 Marks)

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