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**Fourth Semester B.E. Degree Examination, December 2010**  
**Computer Organization**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting at least TWO questions from each part.**

**PART – A**

- 1 a. What is a stored program concept? Explain the functional units of a stored program digital computer, along with a block diagram. (10 Marks)
- b. Define the following terms:  
 i) Processor clock                      ii) RISC                      iii) SPEC rating  
 iv) Basic performance equation      v) the stack frame (10 Marks)
- 2 a. Represent the decimal values 5, -2 and -10 in the following binary formats:  
 i) Sign and magnitude    ii) 1's complement    iii) 2's complement. (06 Marks)
- b. Registers  $R_1$  and  $R_2$  of a computer, contain the decimal values 1200 and 4600. What is EA of the memory operand in each of the following instructions?  
 i) Load  $20(R_1), R_5$   
 ii) MOVE #3000,  $R_5$   
 iii) Store  $R_5, 30(R_1, R_2)$   
 iv) Add  $-(R_2), R_5$   
 v) Subtract  $(R_1)+, R_5$  (05 Marks)
- c. Consider the following possibilities for saving the return address of a subroutine:  
 i) In a processor register  
 ii) In a memory location  
 iii) On a stack  
 Which of these possibilities support the subroutine nesting and which support subroutine recursion? (09 Marks)
- 3 a. What is an interrupt? Explain polling and vectored interrupts with their advantages and disadvantages. (08 Marks)
- b. What is DMA? What are its advantages? With the supporting diagram, explain different registers in a DMA interface. (06 Marks)
- c. What is bus arbitration? Explain the centralized arbitration, with a neat diagram. (06 Marks)
- 4 a. What is a synchronous bus? Explain the timing of an input transfer on a synchronous bus with a timing diagram. (06 Marks)
- b. Define:  
 i) Cycle stealing  
 ii) burst mode  
 iii) Full handshake  
 iv) Plug-and-play (08 Marks)
- c. What are the interface circuits? Explain a general 8-bit parallel interface, with a neat diagram. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.  
 2. Any revealing of identification, appeal to evaluator and /or equations written eg,  $42+8=50$ , will be treated as malpractice.

PART - B

- 5 a. Explain the synchronous DRAM, with a neat diagram. (10 Marks)
- b. What is a cache? Explain any two cache mapping functions. (10 Marks)
  
- 6 a. What are the replacement algorithms? Briefly explain the LRU replacement algorithm. (08 Marks)
- b. What is a virtual memory? With a neat block diagram, explain the virtual memory address translation. (08 Marks)
- c. Briefly explain the controller's major functions on the disk drive side. (04 Marks)
  
- 7 a. With a neat diagram, explain the floating point addition/subtraction unit. (10 Marks)
- b. With a neat block diagram, explain the 4-bit carry-lookahead adder. (10 Marks)
  
- 8 a. Explain the 3-bus organization of the data path with a neat diagram and write the control sequence for the instruction ADD R4, R5, R6 for the 3-bus organization. (10 Marks)
- b. With a neat block diagram, explain the hardwired control unit. (10 Marks)

